WE CLAIM:

1. A cache, having a number of sets and ways, the cache comprising a plurality of addressable banks, each bank populated by clusters of memory cells, wherein the clusters within one of the banks are associated with fewer than the total number of ways in the cache.

2. The cache of claim 1, wherein the clusters within each bank are associated with only one way.

3. The cache of claim 1, wherein the clusters within each bank are associated with two ways.

4. The cache of claim 1, wherein the clusters within each bank are associated with half the total number of ways in the cache.

5. The cache of claim 1, wherein the banks have a number of clusters equal to number of bits stored by a cache line of the cache.

6. A power control method in an integrated circuit, comprising, in response to a microinstruction, disabling predetermined modules within an internal cache.

7. The power control method of claim 6, wherein, in response to an evict microinstruction, all ways of the internal cache are disabled except for a victim way.

8. The power control method of claim 6, wherein, in response to a tag inquiry microinstruction, data fields of the internal cache are disabled.

9. The power control method of claim 6, wherein, in response to a tag and data read microinstruction, all ways are disabled except a target way.

10. The power control method of claim 6, wherein, in response to a tag write microinstruction, data fields of all cache entries are disabled .

11. The power control method of claim 6, wherein, in response to a tag write microinstruction, all ways are disabled except a target way.

12. The power control method of claim 6, wherein, in response to a tag write/data read microinstruction, data fields throughout the cache are disabled.

13. The power control method of claim 6, wherein, in response to a tag write/data read microinstruction, all ways are disabled except a target way.

14. The power control method of claim 6, wherein, in response to a tag and data write microinstruction, all ways are disabled except a target way.

15. The power control method of claim 6, wherein, in response to a data write microinstruction, tag fields throughout the cache are disabled.

16. The power control method of claim 6, wherein, in response to a data write microinstruction, all ways are disabled except a target way.

17. The power control method of claim 6, wherein, in response to a tag invalidate microinstruction, tag fields and data fields throughout the cache may be disabled.

18. The power control method of claim 6, wherein, in response to a tag invalidate microinstruction, all ways are disabled except a target way.

19. The power control method of claim 6, wherein a victim allocation unit is disable in response to a microinstruction selected from the group of: a tag and data read microinstruction, a tag write microinstruction, a tag and data write microinstruction, a data write microinstruction, a tag invalidate microinstruction,

20. A cache control method comprising:
in response to a data request, generating at least one microinstruction within a cache,
disabling predetermined portions of the cache based on the microinstruction.

21. The cache control method of claim 20, wherein, when the data request is a read request:
a first microinstruction causes data to be read from all ways in the cache, and
if the read request hits the cache, a second microinstruction causes data to be read from a target way, all other ways being disabled during the second microinstruction.

22. The cache control method of claim 21, further comprising:
reading data from a victim allocation unit during the first microinstruction and
disabling the victim allocation unit during the second microinstruction.

23. The cache control method of claim 20, wherein, when the data request is a data replacement request, a microinstruction causes data to be written to a tag field and data field in a single way, all other ways being disable during the microinstruction.

24. The cache control method of claim 20, wherein, when the data request is a write request made pursuant to an eviction from a higher level cache:

a first microinstruction causes data to be read from tag fields from all ways of the cache, all other fields in the ways being disabled during the first microinstruction, and

if the data request hits the cache, a second microinstruction may energize a tag field and data field of a matching way, all other ways being disabled during the second instruction.

25. The cache control method of claim 20, wherein, when the data request is a cache writeback invalidate instruction:

a first microinstruction causes a victim way to be enabled, all other ways being disabled during the first microinstruction, and

if an addressed cache entry in the victim way stores valid data, a second microinstruction causes data to be written in a state field of the cache entry, all other ways being disabled during the second microinstruction.

26. The cache control method of claim 24, wherein all other fields of the cache entry are disabled during the second microinstruction.

27. The cache control method of claim 20, wherein, when the data request is a cache invalidate request, a microinstruction causes data to be written in a state field of an addressed cache entry in a target way, all other ways being disabled during the microinstruction.

28. The cache control method of claim 27, wherein all other fields of the cache entry are disabled during the microinstruction.

29. The cache control method of claim 20, wherein, when the data request is a write pursuant to a read-for-ownership request issued by higher level cache, a microinstruction causes data to be written in a tag field and a state field of an addressed cache entry in a target way, all other ways being disabled during the microinstruction.

30. The cache control method of claim 29, wherein all other fields of the addressed cache entry are disabled during the microinstruction.

31. The cache control method of claim 20, wherein, when the data request is a snoop probe, a microinstruction causes data to be read from tag fields and state fields through all ways in the cache, all other fields throughout the cache being disabled during the microinstruction.

32. The cache control method of claim 31, wherein, if the data request hits the cache and state data of a matching cache entry represents exclusive state, a second microinstruction causes data to be written to a state field of the matching cache entry, all other ways are disabled during the second microinstruction.

33. The cache control method of claim 31, wherein, if the data request hits the cache and the snoop probe is not a Go-to-Shared snoop, a second microinstruction causes data to be written to a state field of the matching cache entry, all other ways are disabled during the second microinstruction.

34. The cache control method of claim 20, wherein, when the data request is a snoop confirm request with associated data, a microinstruction causes data to be read from a data field of a cache entry in a single way and data to be written to a state field of the cache entry, all other ways are disabled during the microinstruction.

35. The cache control method of claim 20, wherein, when the data request is a snoop confirm request with no associated data, a microinstruction causes data to be written to a state field of a cache entry in a single way, all other ways are disabled during the microinstruction.

36. A cache, comprising:

a plurality of cache entries organized into sets and ways,

each cache entry comprising a tag field, a data field and a state field, each of the fields coupled to a respective clock line,

a cache manager, and

a plurality of transmission gates, one provided on each clock line, each connected to the cache manager.

37. The cache of claim 36, further comprising:

a victim allocation unit coupled to another clock line,

another transmission gate provided on the other clock line and connected to the cache manager.